

FIG. 1 is a block diagram of a system 10 in accordance with the present invention. The system 10 includes a host CPU 20, a network switch chip 12, and an FPGA 34. The host CPU 20 is connected to the network switch chip 12 via a bus 22. The network switch chip 12 includes a PCI interface 18 and a FIFO (1526 Bytes) 32. The network switch chip 12 is connected to the FPGA 34 via an expansion bus 36. The FPGA 34 includes a FIFO (1526 Bytes) 32 and a set of registers 34. The registers 34 include ERXD2, ERX_CLK, ERX_INFO2, ERX_SB2, ERX_REQ2, ETX_CLK, ETX_INFO2, ETX_SB2, ETX_GNT2, and ETXD2. The network switch chip 12 also includes a set of registers 16, which include ETXD1, ETX_CLK, ETX_INFO1, ETX_SB1, ETX_GNT1, ERX_CLK, ERX_INFO1, ERX_SB1, ERX_REQ1, and ERXD1. The network switch chip 12 is also connected to an expansion bus 36, which is labeled as Expansion Bus, 36.

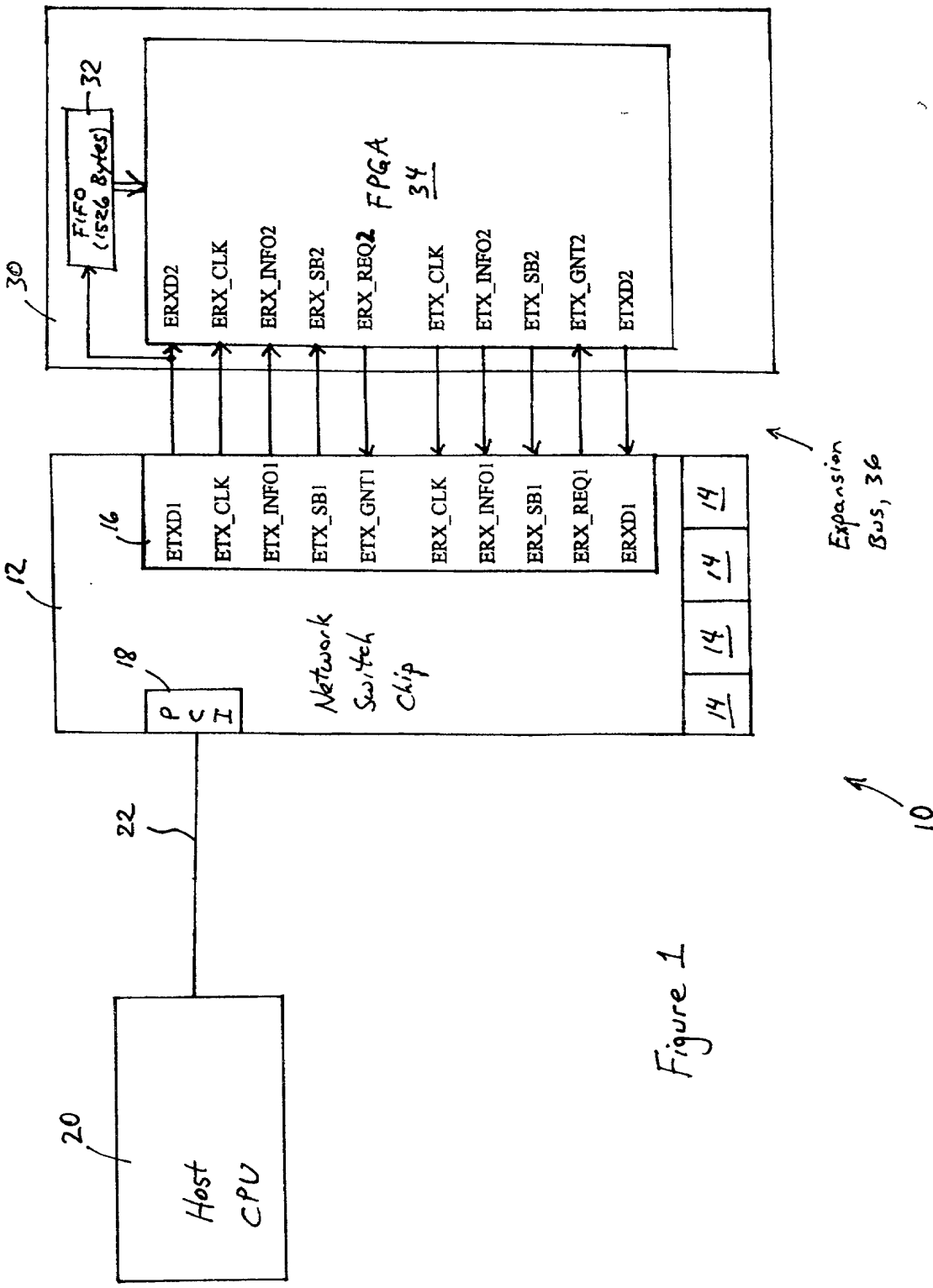


Figure 1

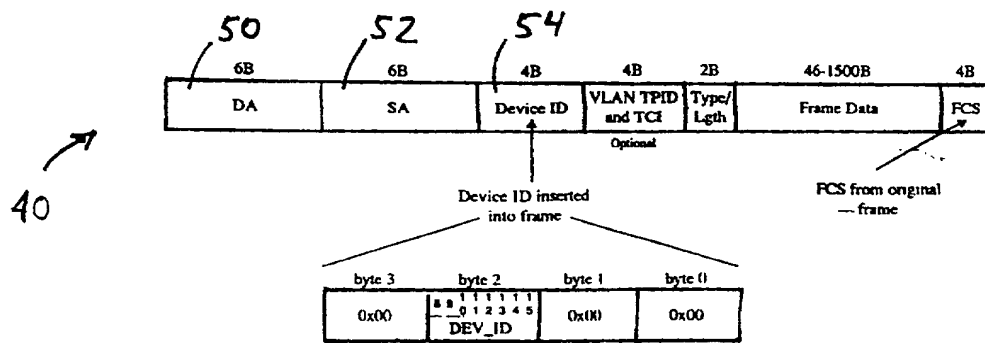


Figure 2

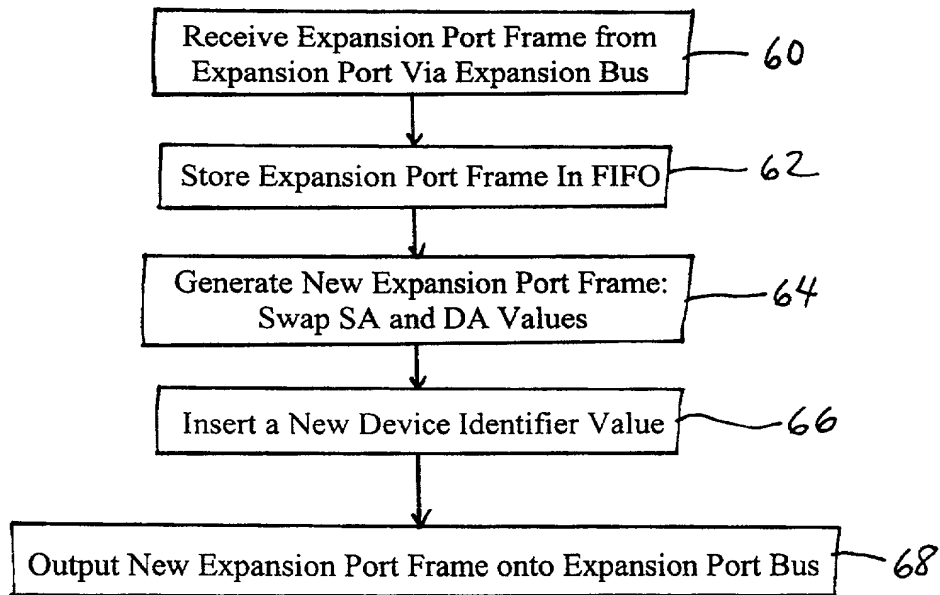


Figure 3